

Exhibit C

Trials@uspto.gov
571-272-7822

10631

Paper 11

Date: August 1, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00455
Patent 9,858,215 B1

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

IPR2023-00455
Patent 9,858,215 B1

I. INTRODUCTION

A. *Background*

Samsung Electronics Co., Ltd. (“Petitioner”) filed a petition for *inter partes* review (Paper 1 (“Pet.” or “Petition”)) challenging claims 1–29 of U.S. Patent 9,858,215 B1 (Ex. 1001 (“’215 patent”)). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). With our authorization (Ex. 3001), Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 9), and Patent Owner filed a Sur-reply to Petitioner’s Preliminary Reply (Paper 10).

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons explained below, we institute an *inter partes* review of all challenged claims on all grounds raised in the Petition.

B. *Related Matters*

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including the following: *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex.) (“the district court litigation”); and IPR2023-00454, which involves U.S. Patent No. 11,093,417 B2, which claims priority to the ’215 patent. Pet. 1–3; Paper 4 at 1–3.

IPR2023-00455

Patent 9,858,215 B1

C. Real Parties in Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the real party in interest. Paper 4 at 1.

D. The '215 Patent and Illustrative Claim

The '215 patent relates to memory modules having ranks of memory. Ex. 1001, code (57). Claims 1 and 21 are independent, and claim 1 is reproduced below.

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is

IPR2023-00455

Patent 9,858,215 B1

not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

E. Asserted Grounds of Unpatentability

Petitioner presents the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–29	103(a)	Perego, ¹ JESD79-2 ²
1–29	103(a)	Perego, JESD79-2, Ellsberry ³
1–29	103(a)	Perego, JESD79-2, Halbert ⁴
1–29	103(a)	Perego, JESD79-2, Matsui ⁵

¹ US 7,363,422 B2, issued Apr. 22, 2008 (Ex. 1071).

² Joint Electron Devices Engineering Council (JEDEC) DDR2 SDRAM Specification (JESD79-2), September 2003 (Ex. 1064).

³ US 2006/0277355 A1, published Dec. 7, 2006 (Ex. 1073).

⁴ US 7,024,518 B2, issued Apr. 4, 2006 (Ex. 1078).

⁵ US 2003/0039151 A1, published Feb. 27, 2003 (Ex. 1082).

II. ANALYSIS

A. *Discretionary Denial*

1. 35 U.S.C. § 314(a)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 314(a) because the factors identified in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”), weigh in favor of denying institution in view of the district court litigation. Prelim. Resp. 53–56.

A Memorandum from Director Vidal titled *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (USPTO June 21, 2022) (“Interim Procedure”)⁶ provides that “the PTAB will not deny institution of an IPR or PGR under *Fintiv* . . . where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” Interim Procedure 9. Petitioner has submitted such a stipulation for all claims in this proceeding, which are all of the claims of the ’215 patent. Ex. 1093; Paper 8 at 1; Paper 9 at 1. Thus, we do not exercise discretion to deny institution under 35 U.S.C. § 314(a).

2. 35 U.S.C. § 325(d)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 325(d) because, according to Patent Owner, the

⁶ Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

IPR2023-00455

Patent 9,858,215 B1

same or substantially the same prior art previously was presented to the Office. Prelim. Resp. 49–53; Paper 10 at 1–4. For the reasons given below, we decline to exercise discretion to deny on this basis.

Section 325 of Title 35 of the United States Code addresses the relationship of proceedings before the Board with other proceedings in the Office, and provides, in part, that

[i]n determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31,^[7] the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.

35 U.S.C. § 325(d).

In evaluating arguments under Section 325(d), we use a two-part framework, determining, first, “whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). If either condition of the first part of the framework is satisfied, we then determine “whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Id.*

Patent Owner argues that “Halbert and Ellsberry, as well as Perego and JEDEC standards . . . , are part of the applicant cited prior art” and, therefore, that the same or substantially the same art was presented previously to the Office. Prelim. Resp. 50–52. Petitioner acknowledges that “Ellsberry and family members of Perego and Halbert were disclosed by

⁷ Chapter 31 (35 U.S.C. §§ 311–319) relates to *inter partes* review.

IPR2023-00455
Patent 9,858,215 B1

Netlist during prosecution,” but Petitioner argues that “they were buried in IDSs with hundreds of other references, and there is no evidence that the Examiner substantively considered those references.” Pet. 135.⁸ Our precedent provides that art disclosed on an IDS is deemed to have been presented previously to the Office. *Advanced Bionics*, Paper 6 at 7–8. Thus, Ellsberry and prior art related to Perego and Halbert were previously presented to the Office. Petitioner’s contentions, however, rely on Perego in combination with JESD79-2, so we consider whether JESD79-2 was presented previously to the Office.

With respect to JESD79-2, Patent Owner argues the following:

[T]he JEDEC standard is also the same as art presented to the office. Petitioner admits as much, stating that “[a] POSITA would have been familiar with these JEDEC standards,” and that “[t]he prior art also refers to these JEDEC standards.” Pet., 9-10 (citing passages from Perego and Ellsberry discussing JEDEC standards), *id.*, 114 (asserting that Ellsberry “expressly incorporates by reference the corresponding JEDEC standards, including JESD79-2 (EX1064)[”]).

Prelim. Resp. 52 (second and third alterations in original). We disagree with Patent Owner. The fact that a person of ordinary skill in the art would have been familiar with JEDEC standards in no way informs us whether those standards were presented to the Office previously. Indeed, the “person of ordinary skill is a hypothetical person who is presumed to be aware of all the pertinent prior art.” *Custom Accessories v. Jeffrey-Allan Industries*, 807 F.2d 955, 962 (Fed. Cir. 1986) (citing *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448, 454 (Fed.Cir.1985)). We do not impute such knowledge to examiners in determining whether art was presented

⁸ When quoting Petitioner’s arguments, we omit the underline emphasis Petitioner included for the names of prior art references.

IPR2023-00455
Patent 9,858,215 B1

previously to the Office. Doing so would essentially eliminate the inquiry given the knowledge that a person of ordinary skill in the art has. We also do not agree with Patent Owner's argument that Perego's and Ellsberry's references to JEDEC standards amount to a previous presentation of those standards to the Office. Although disclosure of a reference on an IDS is sufficient to satisfy the first part of *Advanced Bionics*, as discussed above, we are aware of no precedent (and Patent Owner cites none) that states that any document referenced in or incorporated by reference into a previously presented document is itself considered previously presented.

Thus, based on the record presented, we determine that JESD79-2, on which Petitioner relies, was not presented previously to the Office. Patent Owner does not argue that the same arguments were presented previously to the Office. *See* Prelim. Resp. 49–53.

Because we determine that the first part of the *Advanced Bionics* framework is not satisfied, we decline to deny institution under 35 U.S.C. § 325(d).

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary

IPR2023-00455
Patent 9,858,215 B1

considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art “would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor’s degree in such engineering disciplines and at least three years working in the field” and would have had knowledge of various standards for memory, such as JEDEC, and circuitry used in memories. Pet. 9–10 (citing Ex. 1003 ¶¶ 48–50). Petitioner also contends that “[a]dditional training can substitute for educational or research experience, and vice versa.” Pet. 9 (citing Ex. 1003 ¶ 48).

Patent Owner does not dispute this assessment. *See* Prelim. Resp. 6 (“For purposes of this preliminary response only, Patent Owner applies the skill level proposed by Petitioner.”).

To the extent necessary, and for purposes of this Decision, we accept the uncontested assessment offered by Petitioner, except that we delete the qualifier “at least” to eliminate vagueness as to the amount of experience. The qualifier expands the range indefinitely without an upper bound, and thus precludes a meaningful indication of the level of ordinary skill in the art.

D. Claim Construction

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2022).

Independent claims 1 and 21 recite memory integrated circuits arranged in ranks. Petitioner argues that a “rank” is “an independent set of one or more memory devices on a memory module that act together in

IPR2023-00455

Patent 9,858,215 B1

response to command signals, including chip-select signals, to read or write the full bit-width of the memory module.” Pet. 27–28 (citing Ex. 1003 ¶ 126). Patent Owner does not agree with Petitioner that a rank can include a single memory device but does not otherwise dispute Petitioner’s construction of “rank.” Prelim. Resp. 6–11.

Our analysis focuses on the parties’ dispute about whether a rank may have only one memory device. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

We begin our analysis with the claim language. *In re Power Integrations, Inc.*, 884 F.3d 1370, 1376 (Fed. Cir. 2018) (“Claim construction must begin with the words of the claims themselves.” (internal quotations, brackets, and citation omitted)). Claim 1 recites, in relevant part,

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.

Claim 21 is method claim and recites similar structure in the preamble.

Petitioner cites this claim language in support of its position that a rank can have just one memory device. Pet. 28 (citing Ex. 1001, 37:32–38 (portion of claim reproduced above)). On this record, we determine that the claim language supports Petitioner’s position. Claim 1 recites “at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.” This language is met if there is one

IPR2023-00455
Patent 9,858,215 B1

memory integrated circuit in each rank because “at least one” includes just one.

On this record, we disagree with Patent Owner’s argument that this claim language “do[es] not define the term ‘rank’” but, rather, “provide[s] context that a claimed ‘buffer’ can be, but need not be, coupled to multiple memory devices in the rank.” *See* Prelim. Resp. 9–10. Claim 1 recites “a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus,” and it further recites “enabl[ing] communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer” and “enabl[ing] communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer.” If there is only one memory device in each rank, then the buffer will only be connected to the one memory device in each rank. If two memory devices are the “at least one first memory integrated circuit in the first rank” then the buffer would be “coupled between the [two memory devices] and the memory bus.”

As other intrinsic evidence supporting its position, Petitioner argues that “the 215 Patent describes an embodiment with one memory device in each ‘rank.’” Pet. 29–30 (citing Ex. 1001, 16:66–17:8; Ex. 1003 ¶ 130). Specifically, the ’215 patent states the following:

In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments,

IPR2023-00455

Patent 9,858,215 B1

the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

Ex. 1001, 16:66–17:12.

Patent Owner counters that, “[r]ead in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of the multiple memory devices in the selected rank.” Prelim.

Resp. 11. On this record, we disagree with Patent Owner’s interpretation of this passage. The ’215 patent states that Table 1 is a logic table “for the selection among ranks of memory devices 30 using chip-select signals.”

Ex. 1001, 16:22–24. We see nothing in Table 1 that indicates a further selection of memory devices within each rank. Rather, the passage quoted above indicates an embodiment in which each rank has one memory device because it describes sending the command signal “to only one memory device or the other memory device” by reference to logic showing the selection of one rank or another rank. *See* Ex. 1001, 16:66–17:12.

On this preliminary record, we determine that the intrinsic evidence supports Petitioner’s position that a rank may have only one memory device.

The parties also discuss extrinsic evidence that they say supports their respective positions. *See* Pet. 28–29; Prelim. Resp. 6–8. In light of the intrinsic record discussed above, however, we do not find this evidence to be particularly useful in resolving the parties’ dispute. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (*en banc*) (authorizing the consideration of extrinsic evidence in determining the meaning of claims but noting that it is “in general . . . less reliable than the patent and its prosecution history in determining how to read claim terms”).

IPR2023-00455
Patent 9,858,215 B1

For the reasons discussed above, we preliminarily determine that a rank may have only one memory device. We do not construe the term further at this time. *See Realtime Data*, 912 F.3d at 1375.

*E. Alleged Obviousness over Perego and JESD79-2
(Claims 1–29)*

Petitioner asserts that claims 1–29 are unpatentable as obvious over the combined teachings of Perego and JESD79-2. Pet. 5, 30–112. Patent Owner opposes. Prelim. Resp. 19–33.

1. Overview of the Prior Art

Perego pertains to memory systems and discloses a configurable width buffer device that is coupled to memory devices and allows a data path width to be varied. Ex. 1071, code (57).

JESD79-2 is a JEDEC standard for second generation double data rate (“DDR2”) memory devices. Ex. 1064.

We discuss additional pertinent details of the references in our analysis below.

2. Claim 1

Claim 1 recites a memory module having various components that are configured to operate in a particular manner, which we address in more detail below. To address the subject matter of claim 1, Petitioner relies on Perego’s memory module disclosures in combination with JESD79-2’s disclosures of DDR2 memory operations. Pet. 30–80. Petitioner argues that a person of ordinary skill in the art would have been motivated to combine the teachings of Perego and JESD79-2 because Perego discloses that its memory modules can use DDR2 memory devices and “the JEDEC standard for DDR2 memory devices is JESD79-2.” Pet. 32 (citing Ex. 1071,

IPR2023-00455
Patent 9,858,215 B1

3:62–4:12, 8:1–4, 10:54–67; Ex. 1064); *see also* Pet. 32–35 (further explaining rationale to combine).

Patent Owner argues that JEDEC79-2’s memory organization is incompatible with Perego’s “Rambus-style memory organization.” Prelim. Resp. 24–28. Patent Owner argues that these are “two distinct approaches” and cites extrinsic evidence allegedly showing that Rambus memories lack a chip select network. Prelim. Resp. 25–26 (citing Ex. 1069, 9, 11, 12); *see also* Prelim. Resp. 27 (“Modifying Perego to fit into the JEDEC framework that has fixed ranks and fixed bandwidth would require changing the fundamental operating principle of Perego, which is evidence of non-obviousness.”).

On this record, we are sufficiently persuaded by Petitioner’s argument that a person of ordinary skill in the art would have combined the teachings of Perego and JESD79-2. As Petitioner correctly points out (Pet. 32), Perego discloses using DDR2 memory devices. Ex. 1071, 10:56–59 (“Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices.”). On this record, we find this teaching to use DDR2 sufficiently supports Petitioner’s rationale to combine Perego with JESD79-2, which is the JEDEC DDR2 SDRAM Specification. Ex. 1064, 1 (cover page); *see also* Prelim. Resp. 44 (parenthetical noting that “JESD79-2 is a specification for individual DDR2 SDRAMs”). As to Patent Owner’s argument that Rambus memories lack a chip select network (Prelim. Resp. 25–26), the reference on which Patent Owner relies discloses that chip select information is still used in the particular Rambus devices described. *See* Ex. 1069, 11 (“[I]n the Rambus bus organization, all addresses, commands, data, and chip-select information are sent on the same bus lines.”), 12

IPR2023-00455
Patent 9,858,215 B1

("[T]he example system uses a total of nine (9) lines to carry all necessary information, including addresses, commands, chip-select information, and data."). Thus, on this record, Patent Owner's focus on the lack of a chip select network, which is not recited in the claims of the '215 patent, appears misplaced. We address Patent Owner's more specific arguments below in the discussion of individual claim recitations.

a) Preamble

The preamble of claim 1 recites the following:

A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising.

Petitioner argues that Perego's Figures 3B, 3C, 4A, 4B, and 4C show memory modules that communicate data with a memory controller of a computer system via a bus. Pet. 35–41. For the recited memory commands, Petitioner cites Perego's disclosure of storing and retrieving data in response to commands and argues that a person of ordinary skill in the art would have understood from JESD79-2 that a read or write command can be followed by a subsequent command. Pet. 42–44 (citing Ex. 1071, 3:64–4:12, 7:56–59, 8:1–4, 10:56–58; Ex. 1064, 24–33; Ex. 1003 ¶¶ 229–239). Petitioner cites JESD79-2's disclosure of burst memory operations and argues that a person of ordinary skill "would have understood that Perego's modules were designed to perform multiple read and write operations and output or receive corresponding bursts of data signals, and would have been

IPR2023-00455
Patent 9,858,215 B1

motivated to apply the teachings of JESD79-2 to Perego's module." Pet. 44–46 (citing Ex. 1064, 12, 25–32; Ex. 1003 ¶¶ 233–235, 238).

Apart from its argument that Perego and JESD79-2 would not be combined, which we address above, Patent Owner does not dispute Petitioner's contentions for the preamble.

On this record, we are sufficiently persuaded by Petitioner's contentions for the preamble, and, for purposes of institution, we need not decide whether the preamble is limiting.

b) Printed Circuit Board

Claim 1 recites "a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system." Petitioner argues that Perego's disclosure of including memory modules on printed circuit boards (PCBs) with connectors (such as connectors 390a in Figure 3C) teaches this subject matter. Pet. 46–47 (citing Ex. 1071, 5:56–6:11, 7:39–41, Figs. 3B, 3C; Ex. 1003 ¶¶ 243–248). Petitioner also argues that a person of ordinary skill in the art would have understood that Perego's memory modules could be implemented in a standard dual in-line memory module (DIMM), which would use a PCB with edge connections. Pet. 47–48 (citing Ex. 1071, 3:25–28, 6:34–43; Ex. 1069, 2; Ex. 1062, 29, 66; Ex. 1003 ¶ 247).

Patent Owner does not dispute Petitioner's contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner's contentions for this limitation.

IPR2023-00455
Patent 9,858,215 B1

c) Register

Claim 1 recites “a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command.” Petitioner argues that Perego teaches this subject matter by its disclosure of buffer devices in the memories receiving control and address information for memory operations. Pet. 48–54 (citing Ex. 1071, 5:6–15, 6:12–33, 8:1–4, 9:50–60, 10:56–59, 11:8–12, 13:54–59, Figs. 3B, 4A, 4B, 5A, 5B, 5C; Ex. 1062, 12; Ex. 1064, 26, 29, 49; Ex. 1003 ¶¶ 251–253, 256–258).

Patent Owner does not dispute Petitioner’s contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner’s contentions for this limitation.

d) Ranks

Claim 1 recites

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.

Petitioner argues that Perego teaches memory circuits arranged in ranks by disclosing groups of memory devices that are accessed together in a memory operation. Pet. 54–62 (citing Ex. 1071, 2:4–6, 3:62–4:3, 4:19–22, 6:12–24, 8:1–4, 10:56–58, 14:10–40, 17:22–28, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 261–282). For example, Perego discloses

IPR2023-00455

Patent 9,858,215 B1

“grouping memory devices into multiple independent target subsets (i.e. more independent banks).” Ex. 1071, 15:37–45, *quoted in* Pet. 56.

Petitioner provides the version of Perego’s Figure 3C below.

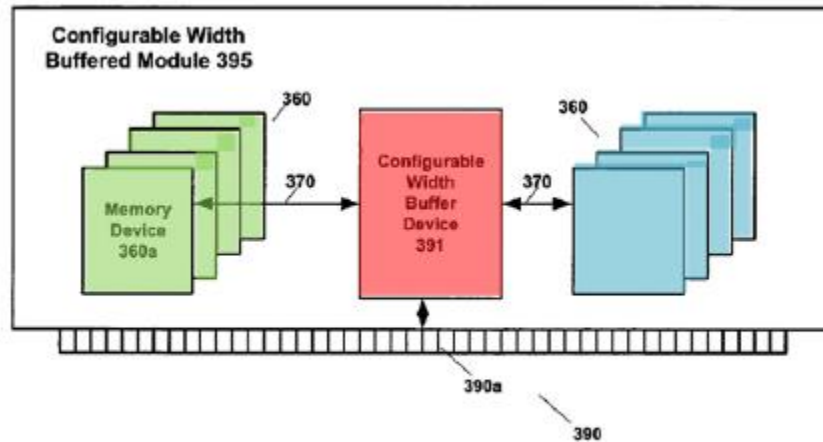


Fig. 3C

Pet. 54, 60. Perego’s Figure 3C above is a block diagram of configurable width buffered module 395 having configurable width buffer device 391 (shaded red) connected on each side via channels 370 to multiple memory devices 360 (shaded green on the left and blue on the right). Ex. 1071, 2:43–45, 7:30–34; Pet. 54, 60. Noting Perego’s disclosure that “one or more of channels 370” can be used in an operation (Ex. 1071, 6:12–24), Petitioner argues that, “when Perego’s buffer device has two channels, and each channel is connected to one rank, Perego’s module includes two ranks of memory devices (green and blue . . .).” Pet. 59–60 (citing Ex. 1003 ¶ 269).

Petitioner also points to Perego’s disclosure of a configurable width buffer having interfaces that may be programmed to have a 64-bit width by connecting to multiple devices having a total width of 64 bits. Pet. 57–58 (citing Ex. 1071, 14:10–15, Figs. 5A, 5B). Petitioner argues that “Perego teaches that the data width accessed in a memory transaction (W_A), and the data width of the buffer interfacing with the memory controller (W_{DP}), can

IPR2023-00455
Patent 9,858,215 B1

both be the same (e.g., both 64 bits), such that the ratio $W_A/W_{DP} = 1:1$.” Pet. 59 (citing Ex. 1071, 14:16–40, 17:22–28, Fig. 5C; Ex. 1003 ¶ 267). According to Petitioner, a person of ordinary skill in the art “would understand that W_A refers to the bit-width of each ‘rank’ of memory devices (e.g., 64 bits can be read or written at a time) when only ‘*one*’ of the ‘one or more channels 370’ . . . is used for a read or write operation.” Pet. 59 (citing Ex. 1071, 6:12–24, 14:23–27, Fig. 3C; Ex. 1003 ¶¶ 268–269).

Petitioner also argues that “it would have been obvious to a [person of ordinary skill in the art] to arrange Perego’s DDR memory devices into ‘ranks,’ and a [person of ordinary skill in the art] would have been motivated to do so, in light of the JEDEC standards.” Pet. 62 (citing Ex. 1064, 6; Ex. 1062, 13, 27–30; Ex. 1003 ¶¶ 273–275). Petitioner relies on JESD79-2’s disclosure of chip select signals for ranks. Pet. 62 (citing Ex. 1064, 6; Ex. 1003 ¶¶ 273–275; Ex. 1062, 13).

Patent Owner argues that Perego does not teach “ranks” of memory devices. Prelim. Resp. 19–24. According to Patent Owner, “Petitioner has not provided any competent evidence that the devices connected to a single channel or interface ‘act together’ in response to a single read/write command.” Prelim. Resp. 21; *see also* Prelim. Resp. 26 (“***Perego’s devices operate on an individual basis***, and do not ‘act together’ as required by the concept of ‘rank.’”). On this record, we disagree with Patent Owner.

Perego discloses that each of the interfaces in configurable width buffer device 391 of Figure 5B, on which Petitioner relies (Pet. 57–59), may connect to multiple devices, resulting in a width of 64 bits. Ex. 1071, 14:12–15; *see* Pet. 57–58 (discussing this disclosure). In particular, Perego discloses that “interfaces 520a and 520b may be programmed to connect to 16‘x4’ width memory devices, 8‘x8’ width memory devices or 4‘x16’ width

IPR2023-00455
Patent 9,858,215 B1

memory devices.” Ex. 1071, 14:12–15; *see* Pet. 57–58 (discussing this disclosure). Perego explains that the “maximum memory device access width” is “the largest number of bits that can be accessed in a *single memory device transfer operation* to or from configurable width buffer device 391.” Ex. 1071, 14:23–27 (emphasis added). Perego also discloses that a memory operation may occur on one of channels 370. Ex. 1071, 6:12–24; *see* Pet. 59 (discussing this disclosure). On this record, in view of Perego’s disclosures, we are sufficiently persuaded that, when there are multiple memory devices that account for the memory device access width (e.g., 64 bits), then those devices “act together” as in Petitioner’s proposed construction. *See* Pet. 27–28. Furthermore, Perego discloses a serialization ratio of 1:1, meaning that the memory device access width (W_A) and the configured buffer device interface width (W_{DP}) are the same. Ex. 1071, 14:32–40, 17:22–28. In such a configuration, each rank would match the full bit-width of the memory module as in Petitioner’s proposed construction. *See* Pet. 27–28.

Patent Owner also argues that Petitioner’s contentions fail because Petitioner’s “definition for a rank requires the use of chip-select signals” but Perego “never mentions ‘chip-select’ signals, lines or the []like.” Prelim. Resp. 24. Petitioner, however, relies on JESD79-2 for its disclosure of chip select signals (*see* Pet. 62), and, as noted above in § II.E.2, we are sufficiently persuaded by Petitioner’s argument that a person of ordinary skill in the art would have combined the teachings of Perego and JESD79-2 given Perego’s express disclosure of using DDR2, for which the industry specification is JESD79-2.

In addition to its argument that Perego discloses one rank per channel, Petitioner also argues that the memory devices connected to two channels may be considered one rank when the devices on the channels act together.

IPR2023-00455
Patent 9,858,215 B1

Pet. 60–62 (citing Ex. 1071, 21:16–20, Figs. 4B, 4C). For example, Perego discloses, with reference to Figure 4B, that “[a]ny number of channels 415a–415d, for example, two channels 415c and 415d *may transfer information simultaneously* and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.” Ex. 1071, 21:16–20 (emphasis added).

Patent Owner argues that “Petitioner does not explain why channels 415c/d together read or write ***full bit-width of the memory module*** under its own theory, given that if each channel width equals the width of the full module, two channels would have a data width twice that of the memory module.” Prelim. Resp. 29. Petitioner’s contention about using only one channel was in the context of a buffer device with two channels. *See* Pet. 59–60. We understand Petitioner’s contention to be that, when there are more than two channels and memory devices on two channels act together by “transfer[ring] information simultaneously” (Ex. 1071, 21:16–20), then the data accessed in a transaction would equal the bit width of the rank (devices on the two acting channels). *See* Pet. 60–62.

Patent Owner also argues that, “although much of the Petition’s theory relies on the module width to be 64 bits, the data width in Perego’s Figure 4B is 16 bits.” Prelim. Resp. 29–30. Even assuming Patent Owner is correct about Figure 4B, Perego expressly discloses a 64-bit wide embodiment, as discussed above. Ex. 1071, 14:12–15; Pet. 57–58.

Patent Owner also argues that, “in Perego, the number of devices involved in a given transaction is not fixed as in the concept of ‘rank,’ but is dynamically configurable based on operating conditions.” Prelim. Resp. 20 (citing Ex. 1071, 10:22–26, 10:31–33, 14:60–65, 15:31–45, 21:16–28, 21:29–38); *see also* Prelim. Resp. 23–24 (“Nothing in the ‘215 patent or any

IPR2023-00455
Patent 9,858,215 B1

JEDEC documents suggests, however, a rank of memory devices refers to a group of memory devices that is dynamically reconstituted to account for the changing memory bit width.”). Patent Owner, however, does not set forth a construction of “rank” that excludes such dynamic reconfigurability. On this record, it is not clear how a device that can have many configurations, one of which satisfies the limitations of a claim, would not render obvious the subject matter of that claim merely because it is capable of additional configurations.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner’s contentions for this limitation.

e) Receive or Output Data in Response to Memory Commands

Claim 1 recites

wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command.

Petitioner argues that Perego teaches this subject matter because it discloses reading from or writing to a target subset of devices (rank) and also discloses that some devices remain in a standby state such that they are not selected as the target devices. Pet. 63–68 (citing Ex. 1071, 6:21–22, 11:56–61, 15:31–45, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 283–303). For example, Perego discloses “grouping memory devices into multiple independent target subsets (i.e. more independent banks)” and “rout[ing] data from an appropriate source (i.e. target a subset of channels,

IPR2023-00455
Patent 9,858,215 B1

internal data, cache or write buffer).” Ex. 1071, 15:42–45, 11:56–61. Perego also discloses that “two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.” Ex. 1071, 21:16–20.

Apart from its arguments about “ranks,” discussed in the preceding section, Patent Owner does not dispute Petitioner’s contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner’s contentions and evidence that are summarized above, and we need not address Petitioner’s additional arguments based on alternative claim constructions. *See* Pet. 69–72.

f) Buffer

Claim 1 recites “a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus.”

Petitioner argues that Perego’s buffer device “isolat[es] the memory controller from signals interfacing with the memory devices” and, therefore, is a buffer as recited in claim 1. Pet. 73–76 (citing Ex. 1071, 4:38–42, 6:12–15, 7:30–34, 10:59–67, 11:1–7, 13:6–10, 13:18–24, 14:65–15:2, 17:61–63, 18:65–19:3, Figs. 5A, 5B, 5C; Ex. 1003 ¶¶ 304–311).

Patent Owner does not dispute Petitioner’s contentions for this limitation.

On this record, we are sufficiently persuaded by Petitioner’s contentions for this limitation.

IPR2023-00455
Patent 9,858,215 B1

g) *Logic*

Claim 1 recites

logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

Petitioner argues that Perego teaches this subject matter because it discloses that different target memory subsets (ranks) on different channels are selected for different operations such that control signals activate only the channel over which the operation is performed. Pet. 76–80 (citing Ex. 1071, 6:15–25, 11:56–61, 12:9–12, 13:54–59, 21:16–20, Figs. 5A, 5B; Ex. 1003 ¶¶ 312–324). Petitioner further argues that a person of ordinary skill in the art

would have understood that, because interfaces 520a/b, 510, and 590 include transceivers (e.g., 575), and because multiplexer/demultiplexer circuit 597 (e.g., in 591) contains “multiplexing logic and demultiplexing logic,” Perego’s buffer device includes logic that sends “*control signals*” to the transceivers, multiplexing/demultiplexing circuits, and to the input and output latches to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write operations.

Pet. 80 (citing Ex. 1071, 14:62–15:6, 15:34–40, 17:41–44, 17:61–62, Figs. 5A, 5B; Ex. 1003 ¶¶ 318–319).

Patent Owner argues that the “Petition does not specifically identify what the alleged first and second control signals are.” Prelim. Resp. 30.

IPR2023-00455
Patent 9,858,215 B1

According to Patent Owner, Perego discloses using address bits to select the channel and the necessary components for an operation, “[b]ut there is no showing [in the Petition] that address information is the same as control signals.” Prelim. Resp. 31 (citing Ex. 1071, 15:37–40, 16:62–65). Patent Owner, however, does not propose a construction for the term “control signals,” let alone one that excludes address information, and on this record, we do not understand the term “control signals” to be so limited. Claim 1 recites that the “logic” is “configured to respond to the first memory command by providing first control signals” and “configured to respond to the second memory command by providing second control signals.”

Claim 1 previously recites “first command and address signals representing the first memory command” and “second command and address signals representing the second memory command.” Thus, according to claim 1, the “logic” responds to first and second memory commands, which are represented in part by address signals, and provides control signals. On this record, we see no reason that these control signals must be devoid of address information.

Patent Owner also argues that Petitioner does not show “the second control signals being different from the first control signals,” as recited in claim 1. Pet. 32–33. Addressing Petitioner’s contentions regarding multiplexing and demultiplexing operations performed, respectively, during read and write operations (*see* Pet. 80), Patent Owner argues that the cited disclosures “do[] not say what the control signals are or how they differ when used with multiplexing and demultiplexing logics” and are “silent on the type of control signals used.” Prelim. Resp. 32 (citing Ex. 1071,

IPR2023-00455
Patent 9,858,215 B1

17:4–44,⁹ 17:61–62, Figs. 5A, 5B). Although those particular disclosures may not disclose particular control signals for the multiplexers and demultiplexers, Petitioner relies on the following disclosure from Perego: “Generally, multiplexer/demultiplexer circuit 597 contains multiplexing logic and demultiplexing logic. The multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations.” Ex. 1071, 17:41–44, *quoted in* Pet. 80. Perego then goes on to explain that “[m]ultiplexer/demultiplexer circuit 597 is configured to use two write control signals W_A and W_B , and two read control signals R_A and R_B ” and that these signals “are based on the selected data path width and bits of the requested memory address or transfer phase.” Ex. 1071, 18:1–6. Thus, Perego discloses write and read *control signals*. On this record, we are sufficiently persuaded by Petitioner’s contentions, including that signals that activate different memory devices on different channels are different. *See* Pet. 77.

We further note that claim 1 is an apparatus claim, and “apparatus claims cover what a device *is*, not what a device *does*.” *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990). Claim 1’s recitation of “the second control signals being different from the first control signals” is a limitation pertaining to the claimed “logic,” which is configured to provide the control signals. On this record, we are sufficiently persuaded that Perego discloses logic that is configured to produce different control signals at least based on whether the operation is a read or a write.

⁹ Petitioner cited column 17, lines 41 through 44, not lines 4 through 44. Pet. 80.

IPR2023-00455
Patent 9,858,215 B1

As to Patent Owner’s argument that “Perego does not mention chip-select signals” (Prelim. Resp. 31), Petitioner relies on JESD79-2 for its disclosure of chip select signals (*see* Pet. 62), as discussed above in § II.E.2.d.

Patent Owner further argues that Petitioner makes “no showing whatsoever that the address information, or the purported chip-select signal, is ever ‘provid[ed] . . . to the buffer.’” Prelim. Resp. 32 (alterations by Patent Owner; citing Pet. 76–80). We disagree because Petitioner asserts that Perego discloses “send[ing] ‘control signals’ to the transceivers, multiplexing/demultiplexing circuits, and to the input and output latches to selectively activate those circuit elements *of the buffer* according to the targeted rank and direction of the read and write operations.” Pet. 80 (emphasis added; Petitioner’s emphasis omitted). Thus, Petitioner argues that the control signals are sent to components of the buffer.

For the reasons discussed above and based on the evidence presented with the Petition, on this record, we are sufficiently persuaded by Petitioner’s contentions for the “logic” limitation of claim 1.

h) Determination for Claim 1

For the reasons discussed above and based on Petitioner’s contentions and evidence, summarized above, we are persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claim 1 is unpatentable as obvious over the combined teachings of Perego and JESD79-2. We note that Petitioner presents a short discussion of alleged secondary considerations of obviousness. Pet. 135. At this stage, Patent Owner does not present evidence of secondary considerations as to any of the challenged claims. Because we are sufficiently persuaded by

IPR2023-00455
Patent 9,858,215 B1

Petitioner’s showing, we need not rely on Petitioner’s assertions of secondary considerations.

3. *Claims 2–29*

Petitioner also asserts that independent claim 21 and dependent claims 2–20 and 22–29 are unpatentable as obvious over the combined teachings of Perego and JESD79-2. Pet. 80–112. Patent Owner relies on the arguments addressed above in § II.E.2 and does not set forth additional arguments for claims 2–29 at this stage of the proceeding. *See* Prelim. Resp. 19–33. We have reviewed Petitioner’s contentions, and we are sufficiently persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claims 2–29 are unpatentable as obvious over the combined teachings of Perego and JESD79-2.¹⁰

F. Additional Grounds

As noted above, Petitioner asserts three additional grounds, each adding one of Ellsberry, Halbert, and Matsui2 to the combination of Perego and JESD79-2 discussed above. Pet. 5, 112–134. Patent Owner opposes. Prelim. Resp. 33–49. Having determined that the Petition meets the threshold for institution (reasonable likelihood of prevailing as to at least one of the challenged claims) based on the Perego and JESD79-2 obviousness ground, the remainder of this Decision focuses on the parties’ disputes to provide guidance to the parties for the trial.

¹⁰ Claim 6 recites, in part, “[t]he memory module of claim 1, further comprising determining a latency value.” Although this claim appears to “conflate[] elements of both an apparatus and a method,” *Samsung Electronics America, Inc. v. Prisia Engineering Corp.*, 948 F.3d 1342, 1355 (Fed. Cir. 2020), we do not view this potential indefiniteness as an impediment to evaluating whether the recited subject matter would have been obvious.

IPR2023-00455
Patent 9,858,215 B1

1. Prior Art Status of Ellsberry

In an *inter partes* review, a petitioner “may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b). Patent Owner argues that “documents are ‘printed publication’ prior art only as of the date they became published and available to the public.” Prelim. Resp. 35–36. Patent Owner argues, therefore, that Ellsberry is not a prior art printed publication under 35 U.S.C. § 311(b) because it was published in December 2006, which is after the effective filing date of July 1, 2005, that Petitioner asserts applies to the ’215 patent. Prelim. Resp. 34; *see* Pet. 5–6 (asserting that the claims of the ’215 patent are not entitled to the benefit of a filing date before July 1, 2005).

We disagree with Patent Owner’s statutory interpretation. Ellsberry is a printed publication, having been published in December 2006, as Patent Owner acknowledges. *See* Ex. 1073, code (43) (publication date of Dec. 7, 2006); *see also* Prelim. Resp. 34 (acknowledging publication date). On this record, we are persuaded by Petitioner’s contentions that Ellsberry is prior art under 35 U.S.C. § 102(e), having been filed “by another . . . in the United States before the invention by the applicant for patent.” *See* Pet. 5–8 (asserting a priority date of no earlier than July 1, 2005, for the ’215 patent); *see also* Ex. 1073, code (22) (filing date of June 1, 2005). Thus, Petitioner asserts a permissible ground of unpatentability under 35 U.S.C. § 311(b) by arguing that claims 1–29 are unpatentable under 35 U.S.C. § 103(a) on the basis of Ellsberry, which is a prior art printed publication, in combination with other prior art.

IPR2023-00455
Patent 9,858,215 B1

2. *Combination of Perego, JESD79-2, and Ellsberry*

Petitioner provides various reasons that a person of ordinary skill in the art would have combined the teachings of Perego, JESD79-2, and Ellsberry. Pet. 112–16. Petitioner relies on various teachings from Ellsberry as additional evidence that certain claimed features would have been obvious to a person of ordinary skill in the art. Pet. 116–26.

Patent Owner argues that Petitioner has not provided sufficient reasoning to combine the teachings of Ellsberry with those of Perego and JESD79-2. Prelim. Resp. 36–42. On this record, we disagree with Patent Owner’s arguments, which we address in turn.

According to Patent Owner, “Petitioner first argues that a [person of ordinary skill in the art] would have combined the two references because they are allegedly analogous art,” which “is insufficient as a matter of law.” Prelim. Resp. 36. Petitioner alleges that Ellsberry is analogous art so that it can be considered for obviousness, but Petitioner’s reason to combine is not simply that Ellsberry is analogous art. *See* Pet. 114–16.

Patent Owner argues that relevance of JEDEC standards is not a reason to combine Ellsberry and Perego because “Perego is not about being JEDEC compliant.” Prelim. Resp. 36; *see also* Prelim. Resp. 41 (“Petitioner does not explain why a [person of ordinary skill in the art] would modify Perego to make it comply with JEDEC.”). For reasons discussed above in § II.E.2, we are sufficiently persuaded that Perego’s disclosure of DDR2 devices supports Petitioner’s rationale to combine with JESD79-2, i.e., a JEDEC DDR2 standard.

Patent Owner next argues that Perego does not use ranks of memory and, therefore, that a person of skill in the art would not have looked to Ellsberry for information on rank multiplication. Prelim. Resp. 37. For the

IPR2023-00455
Patent 9,858,215 B1

reasons discussed above in § II.E.2.d, we are sufficiently persuaded that Perego discloses ranks of memory. Patent Owner further argues that, if Perego discloses ranks, there is no need to look to Ellsberry for teachings on how to target certain devices because Perego discloses its own way of targeting a channel. Prelim. Resp. 37. For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches the subject matter of claim 1, but we also are sufficiently persuaded that a person of ordinary skill in the art would have considered additional relevant teachings, such as those in Ellsberry related to active and non-active chip select signals. *See* Pet. 118–19.

Patent Owner argues that Petitioner “ignores the significant structural differences in Perego and Ellsberry.” Prelim. Resp. 38; *see* Prelim. Resp. 38–41 (additional arguments regarding structural differences in the references). On this record, we do not view any alleged structural differences as an impediment to relying on particular teachings of Ellsberry. Indeed, the Federal Circuit has

consistently held . . . that “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.”

MCM Portfolio LLC v. Hewlett-Packard Co., 812 F.3d 1284, 1294 (Fed. Cir. 2015) (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Patent Owner also argues that “Ellsberry does not cure the deficiency of Perego,” disputing various assertions of Petitioner as to Ellsberry’s disclosure. Prelim. Resp. 42–44 (emphasis omitted). For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of

IPR2023-00455
Patent 9,858,215 B1

Perego and JESD79-2 teaches the subject matter of claim 1, and, therefore, on this record we do not agree with Patent Owner that there are deficiencies in the asserted combination.

3. Combination of Perego, JESD79-2, and Halbert

Patent Owner also argues that “Halbert would not cure the deficiencies of Perego,” disputing various assertions of Petitioner as to Halbert’s disclosure. Prelim. Resp. 45–46. For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches the subject matter of claim 1, and, therefore, on this record we do not agree with Patent Owner that there are deficiencies in the asserted combination.

Patent Owner also argues that Petitioner has not provided sufficient reasoning to combine Halbert with Perego and JESD79-2 and that Petitioner “provides no detail whatsoever on how it suggests a [person of ordinary skill in the art] should incorporate Halbert’s design in Perego.” Prelim. Resp. 47–49. For claim 1, we understand Petitioner to be relying on “Halbert’s disclosure of different ranks on different data paths” to bolster its contention that having multiple ranks would have been obvious, as discussed in the cited testimony of Dr. Wolfe. Pet. 128–129 (citing Ex. 1003 ¶¶ 277–282). We note, however, that Petitioner’s reference to limitations “[1.d.2]-[1.d.3]” is somewhat confusing because the cited testimony from Dr. Wolfe does not appear directed to these limitations, which relate to which rank is selected. On this record, we are sufficiently persuaded by Petitioner’s reasoning that a person of ordinary skill in the art “would have recognized that the combination would have resulted in a predictable variation, which would improve similar devices like Perego in the same way

IPR2023-00455
Patent 9,858,215 B1

and not yield unexpected results or challenges.” *See* Pet. 128 (citing Ex. 1003 ¶ 283).

4. *Combination of Perego, JESD79-2, and Matsui2*

Petitioner relies on Matsui2 only to address limitations of dependent claim 7 relating to an on-die-termination (ODT) circuit that can be turned on and off. *See* Pet. 131–34. Patent Owner argues that “Perego already discloses how to terminate signal lines” and “Petitioner does not explain why those solutions are inadequate.” Prelim. Resp. 49. Petitioner essentially relies on Matsui2 as further evidence for its assertion that it would have been obvious to have an ODT circuit that can be turned on and off (*see* Pet. 92–95), and on this record, we find Petitioner’s reliance on Matsui2 to be sufficiently persuasive.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one claim of the ’215 patent, and we institute *inter partes* review of all challenged claims on all grounds raised in the Petition. *See* 37 C.F.R. 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”). At this stage of the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims or the construction of any claim term.

IPR2023-00455

Patent 9,858,215 B1

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted as to claims 1–29 of the ’215 patent on all challenges raised in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which will commence on the entry date of this decision.

IPR2023-00455

10665

Patent 9,858,215 B1

FOR PETITIONER:

Eliot Williams

Theodore Chandler

Ferenc Pazmandi

John Gaustad

Brianna Potter

BAKER BOTTS LLP

eliot.williams@bakerbotts.com

ted.chandler@bakerbotts.com

ferenc.pazmandi@bakerbotts.com

john.gaustad@bakerbotts.com

brianna.potter@bakerbotts.com

FOR PATENT OWNER:

Hong Zhong

Jonathan Lindsay

IRELL & MANELLA LLP

hzhong@irell.com

jlindsay@irell.com